

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): S. Shukuri, et al.

Appln. No. 10/635,511

Filed: August 7, 2003

For: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE HAVING
DEPOSITED LAYER FOR GATE INSULATION

Group: 2814

Examiner: L. Pham

**INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR § 1.97 AND § 1.98**

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

December 6, 2004

Sir:

Pursuant to Applicants' duty of disclosure, enclosed please find a copy of an Office Action in connection with a Japanese patent application corresponding to the above-identified application. Also enclosed is an English translation of this Office Action. Further enclosed are copies of each of the documents cited in the enclosed Office Action. Moreover, an English-language Abstract is enclosed with each of these cited documents, except for Japanese Patent Document No. 4-122063; a corresponding U.S. patent to No. 4-122063 (that is, U.S. Patent No. 5,241,208 to Taguchi) is enclosed herewith. Also enclosed herewith is an English translation of cited Japanese Patent Document No. 6-61499.

Also enclosed herewith is a copy of Japanese Patent Document No. 9-181159 and an English abstract thereof; and a copy of Japanese Patent Document No. 9-260484, and U.S. Patent No. 5,897,361 corresponding thereto.

Further enclosed herewith is a Form PTO/SB/08A, listing all of the enclosed documents.

This Information Disclosure Statement is being submitted prior to a first Office Action on the merits in the above-identified application. Accordingly, requirements of 37 CFR § 1.97(b)(3) are satisfied.

In any event, the following Statement is made under 37 CFR § 1.97(e):

Each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.

To the extent that the enclosed documents are not in English, it is respectfully submitted that requirements of 37 CFR § 1.98(a)(3) are satisfied by English translations and/or English Abstracts and/or corresponding U.S. patents to the non-English language documents.

In addition, Applicants respectfully submit the following comments, in connection with the enclosed documents.

Japanese Patent Document No. 6-61499 does not disclose an element isolation region formed by forming grooves in a substrate, by depositing an insulating film over the grooves by using a vapor deposition method and by polishing the insulating film so as to fill the insulating film in the grooves. This document does not disclose the gate insulating film including a thermally oxidized film and a deposited film formed over the thermally oxidized film and having a thickness greater than that of the thermally oxidized film. This document discloses a gate insulating film

including a thermally oxidized film of 16 nm thickness and a HTO CVD film of 16 nm and a field oxide film 27, as shown, for example, in Figs. 9-11 and 27.

Japanese Patent document No. 6-244366 does not disclose an element isolation region which is formed by forming grooves in a substrate, by depositing an insulating film over the grooves using a vapor deposition method and by polishing the insulating film so as to fill the insulating film in the grooves. This document also does not disclose a gate insulating film including a thermally oxidized film and a deposited film formed over the thermally oxidized film. This document discloses LOCOS structure 12.

Japanese Patent Document No. 4-122063, corresponding to U.S. Patent No. 5,241,208, does not disclose an element isolation region which is formed by forming grooves in a substrate, by depositing an insulating film over the grooves using vapor deposition methods and by polishing the insulating film so as to fill the insulating film in the grooves. This document does not disclose a gate insulating film including a thermally oxidized film and a deposited film formed over the thermally oxidized film and having a thickness greater than that of the thermally oxidized film. This document discloses a selective oxidation method for forming a field oxide film 9 and a gate insulating film including a thermally oxidized film 16 of 7 nm and a nitride film 17 of 7 nm, as seen in column 4, lines 37-51 and in Fig. 2A of U.S. Patent No. 5,241,208.

Japanese Patent Document No. 10-22397 has a publication date of January 23, 1998, which is later than the priority date under 35 USC §119 of December 9, 1997, of the above-identified application. In any event, No. 10-22397 does not disclose an element isolation region which is formed by forming grooves in

a substrate, by depositing an insulating film over the grooves using a vapor deposition method and by polishing the insulating film so as to fill the insulating film in the groove. This document also does not disclose a gate insulating film including a thermally oxidized film and a deposited film formed over the thermally oxidized film and having a thickness greater than that of the thermally oxidized film. This document discloses LOCOS and a gate insulating film including a thermally oxidized film 3 of 10 nm and a high temperature CVD oxide film 6 of 10 nm.

In view of all of the foregoing, it is respectfully submitted that applicable requirements of 37 CFR § 1.97 and § 1.98 have been satisfied, in connection with each of the documents listed on the enclosed Form. Accordingly, consideration of the listed documents, upon examination of the above-identified application, is respectfully requested.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Deposit Account No. 01-2135 (Case No. 501.36694CV4), and please credit any excess fees to such Deposit Account.

Respectfully submitted,

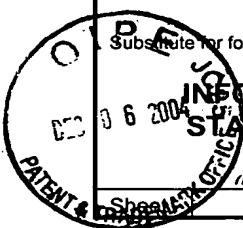
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				Complete if Known		
Application Number		10/635,511				
Filing Date		8/7/2003				
First Named Inventor		S. Shukuri, et al.				
Art Unit		2814				
Examiner Name		P. Long				
Attorney Docket Number		501.36694CV4				
U.S. PATENT DOCUMENTS						
Examiner Initials'	Cite No. ¹	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)				
		US- 5,897,361		4/27/1999	Egawa	
		US- 5,241,208		8/31/1993	Taguchi	

FOREIGN PATENT DOCUMENTS							
Examiner Initials'	Cite No. ¹	Foreign Patent Document		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	Translation/Abstract
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)					
		JP 9-181159		7/11/1997	Matsushita Electric Ind. Co.		X
		JP 9-260484		10/3/1997	Kabushiki Kaisha Toshiba		X
		JP 6-61499		3/4/1994	Mitsubishi Electric Corp.		X
		JP 6-244366		9/2/1994	Sony Corp.		X
		JP 4-122063		4/22/1992	Kabushiki Kaisha Toshiba		X
		JP 8-204142		8/9/1996	Oki Electric Ind. Co., Ltd.		X
		JP 9-107028		4/22/1997	Samsung Electron Co., Ltd.		X
		JP 10-022397		1/23/1998	Ricoh Co., Ltd.		X

TO/SB/08B (04-03)

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		Office Action dated September 28, 2004, in corresponding Japanese Patent Application No. Hei 9-338586	

Examiner Signature	Date Considered
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹Applicant's unique citation designation number (optional). ²Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 120 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing the this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.